REMARKS

The Examiner has noted a clerical error in the oath/declaration with respect to identifying the PCT priority application. Applicant notes that the official filing receipt correctly identifies all priority applications to the satisfaction of the applicant. Thus, no action will be taken at this time unless the Examiner specifically requests such.

The Examiner has objected to independent claims 3 and 9 and their dependent claims because the specification did not appear to be consistent with the drawings. Based on the amendments to the drawings, it is believed this objection is now moot and that the specification and drawings are entirely consistent with one another. Reconsideration and withdrawal of the claim objections is requested.

Applicants have cancelled independent claims 1, 6, and 14 in favor of new claims 18-20. The Examiner had rejected independent claims 1, 6, and 14 under 35 USC 102(e) as being anticipated by Yamauchi (US Pat. Pub. 2003/0002328).

The Examiner notes that Yamauchi teaches an asymmetric SRAM cell that employs first and second types of transistors wherein a first type of transistor can be made weaker than the second type of transistor. Yamauchi describes its asymmetric SRAM cell as being comprised of two unit circuits each unit circuit including a load transistor, drive transistor, and access transistor. The load transistor and drive transistor in each unit circuit form an inverter. To make the SRAM cell asymmetric, Yamauchi weakens all of the transistors in one unit circuit equally with respect to the transistors in the other unit circuit. That is, the load transistor, drive transistor, and access transistor in one unit circuit are all kept at the same strength but that strength can be made weaker than the load transistor, drive transistor, and access transistor of the other unit circuit. The inequality in strength between the two unit circuits gives rise to the asymmetry.

In Applicants' amended claims 18-20, language has been added to clarify that one embodiment of the present invention can individually vary the load transistor, drive transistor, and access transistor within each circuit to achieve asymmetry. Just as in Yamauchi, the load transistor and drive transistor in each circuit form an inverter. Moreover, the specification describes multiple embodiments that vary individual transistors to achieve different results. For instance, in one embodiment of the present invention, the load transistor and access transistor have been varied with respect to the drive transistor within one circuit while just the drive transistor has been varied in the other circuit (See, Fig. 2). Figures 3-12 all illustrate additional embodiments in which the transistors are individually varied within each circuit to each specific results with respect to overall leakage and other performance parameters.

Yamauchi does not describe the concept of individually varying transistors within each unit circuit. Rather, Yamauchi describes keeping the load and drive transistors equivalent with one another within a unit circuit but different from the load and drive transistors of the other unit circuit. This is clearly described in ¶ [0026] and ¶ [0028] of Yamauchi.

Based on the amendments to the claims, it is applicants' belief that Yamauchi does not teach each and every element of independent claims 18-20 of the present invention for the reasons given above. Applicants' request reconsideration and withdrawal of the 35 USC 102(e) as being based on Yamauchi (US Pat. Pub. 2003/0002328).

DEPOSIT ACCOUNT

The Commissioner is authorized to charge any deficiencies of payment associated with this Communication, or to credit any overpayment, to **Deposit Account No. 13-4365**.

Respectfully submitted,

Date: Feb. 8, 2007

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(PRIOR ART)

FIG. 1

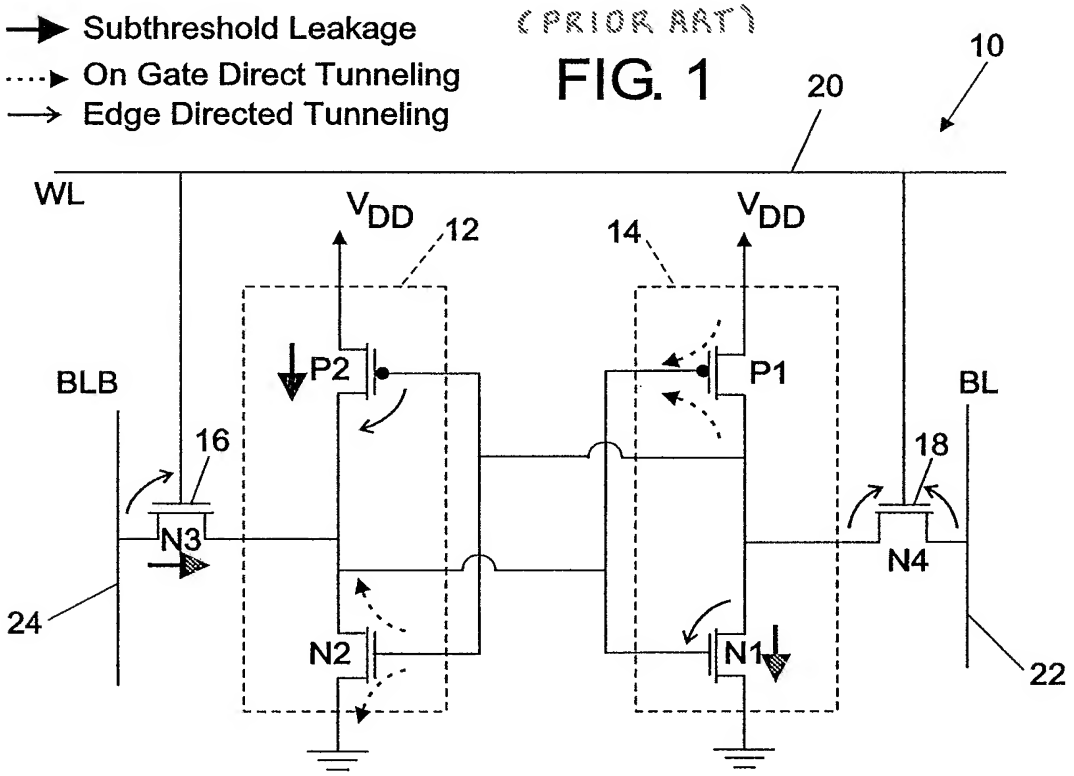
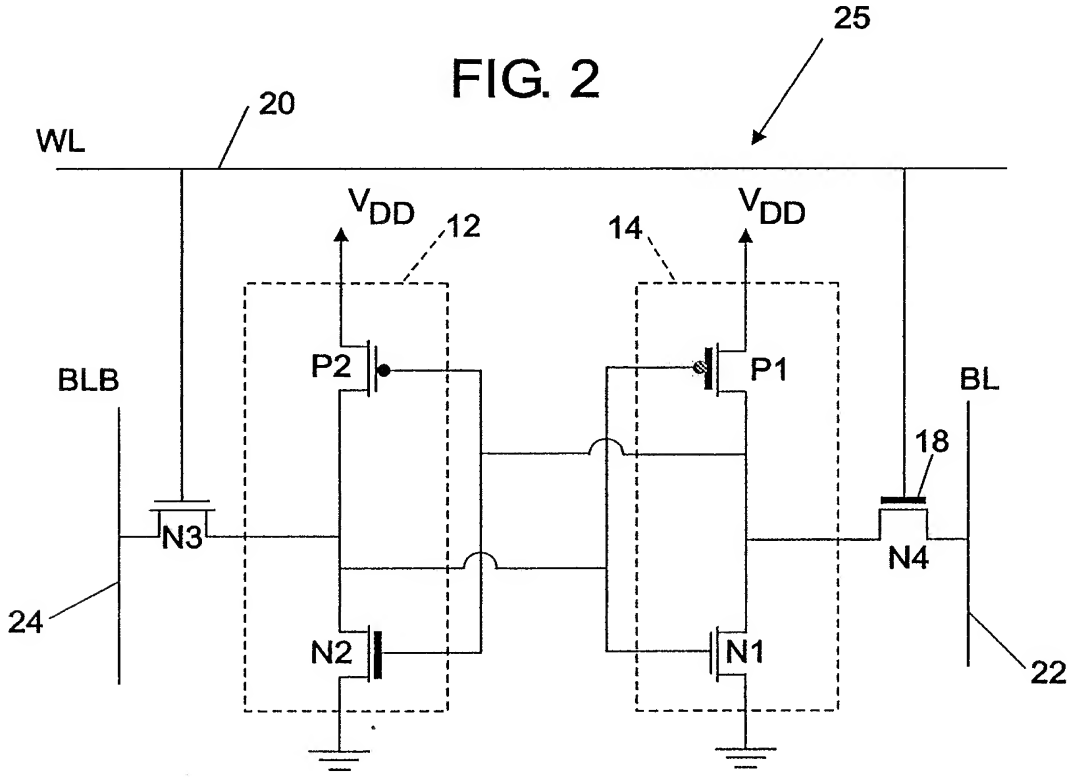


FIG. 2



(PRIOR ART)

FIG. 13

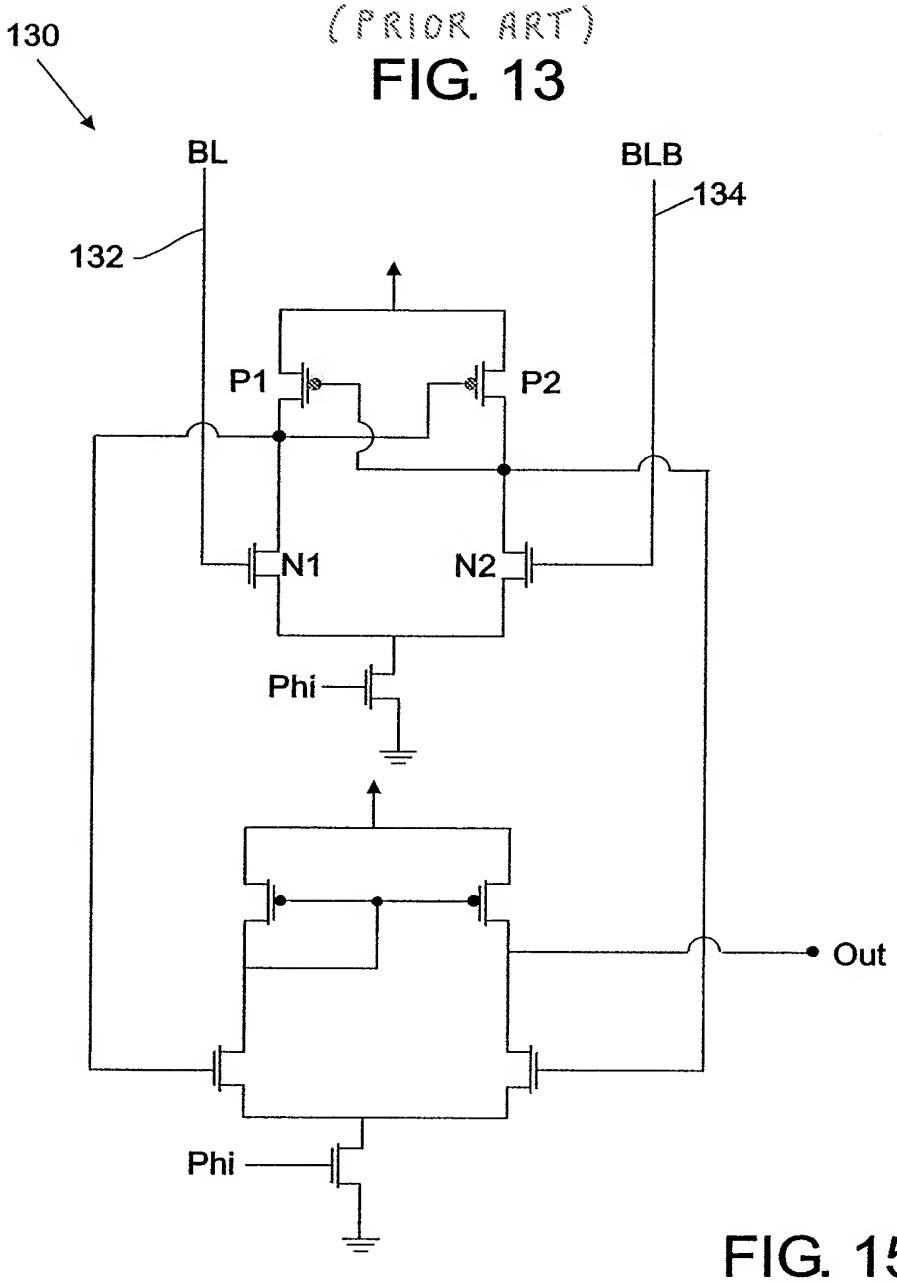


FIG. 15

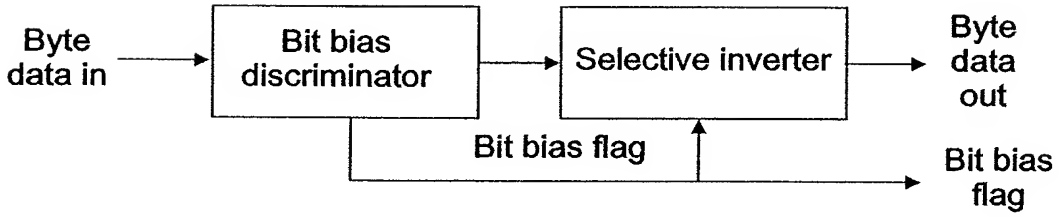
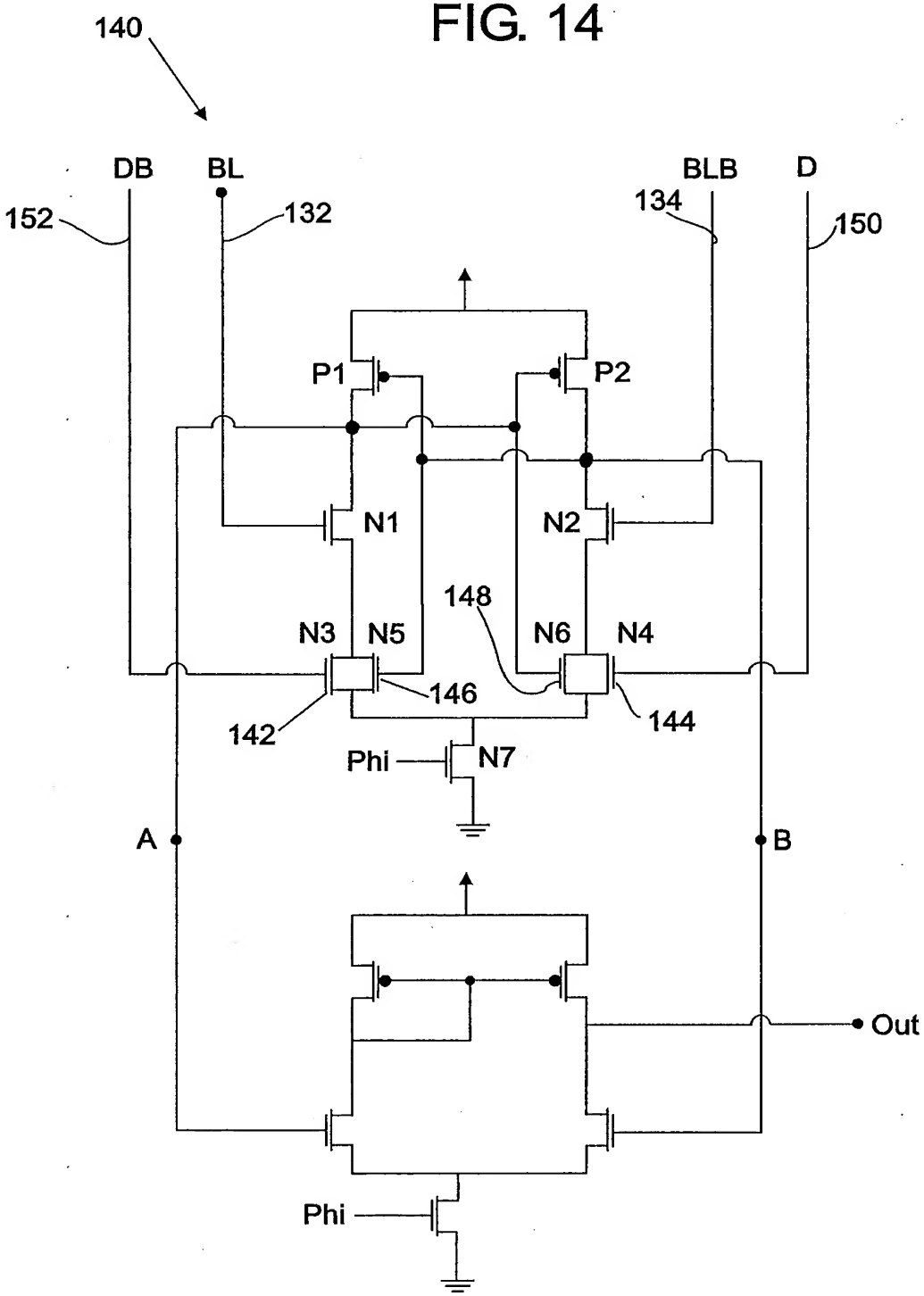


FIG. 14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N2
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N3
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Legend Added

(PRIOR ART)

FIG. 1

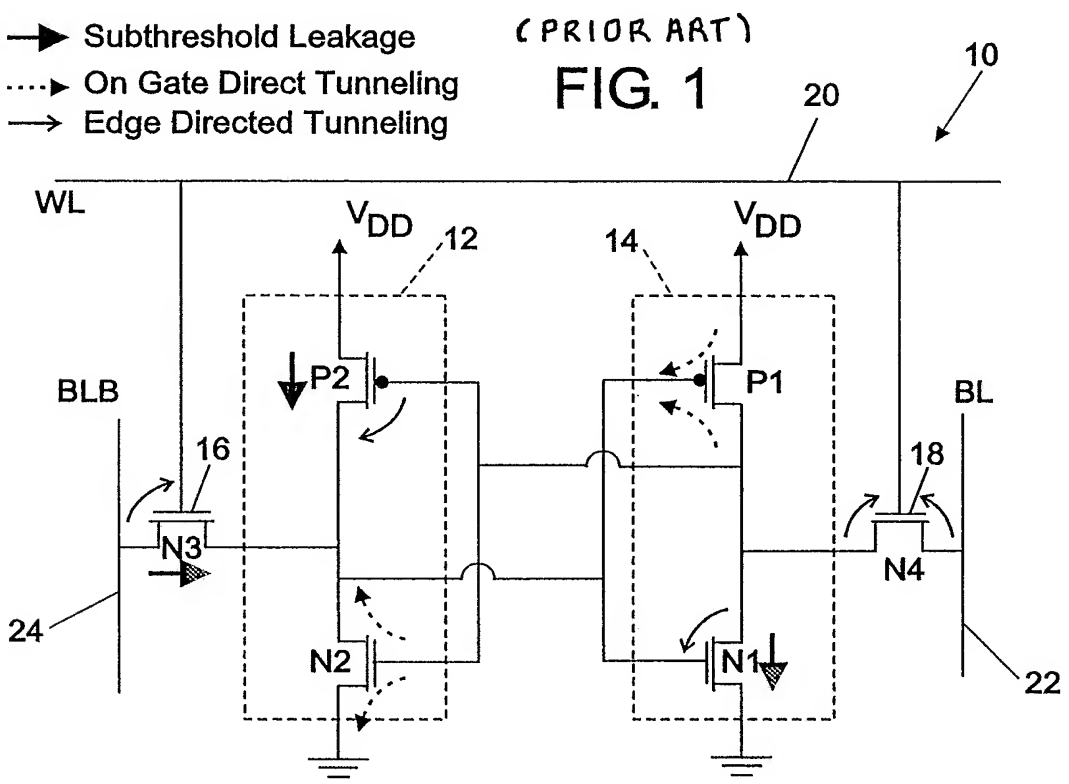
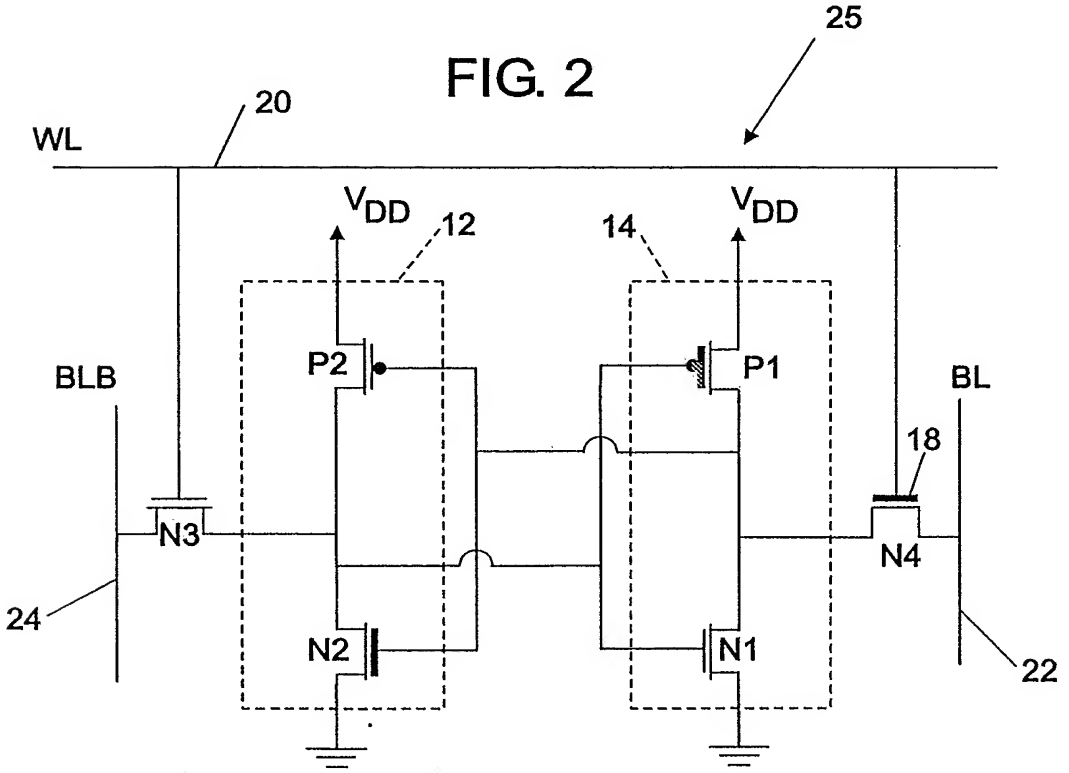


FIG. 2



Legend Added

(PRIOR ART)

FIG. 13

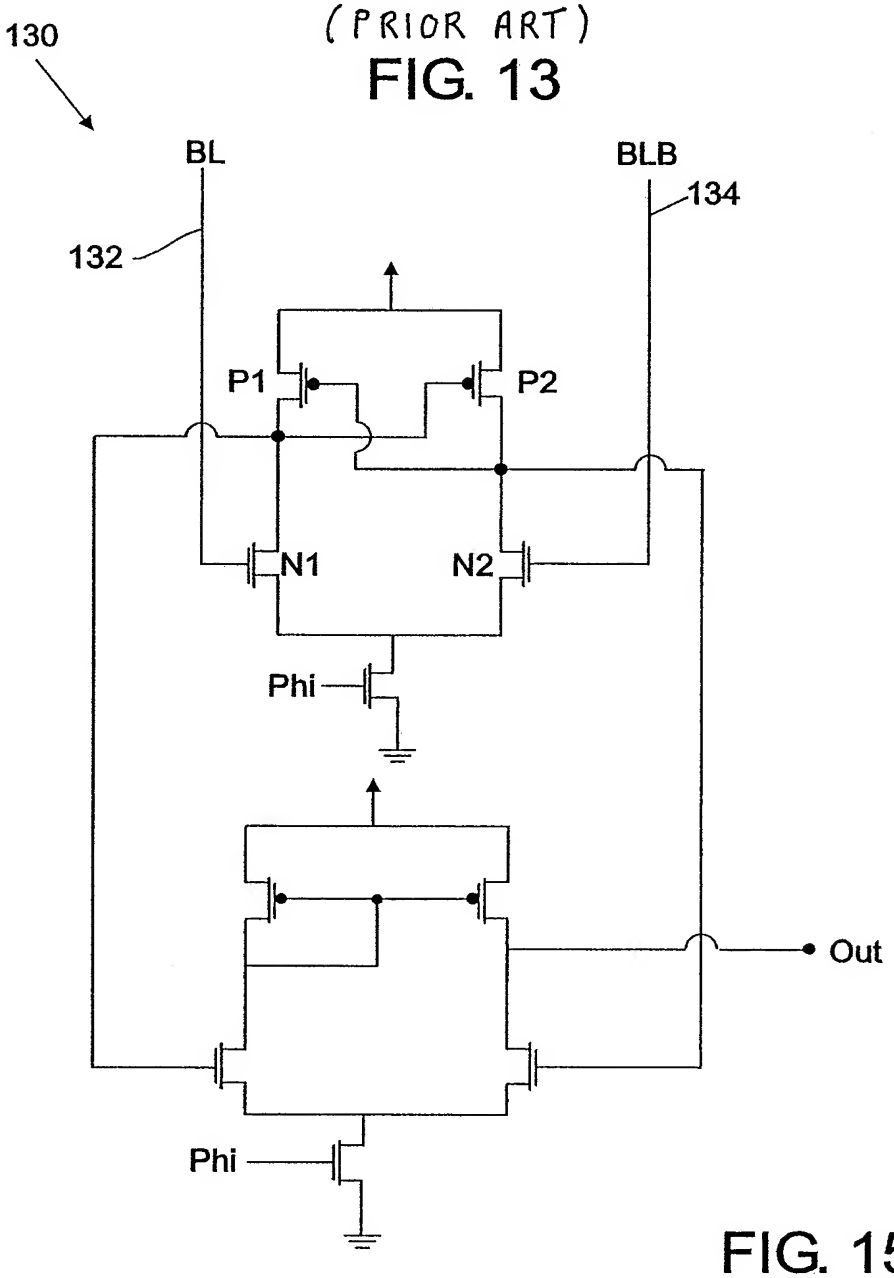


FIG. 15

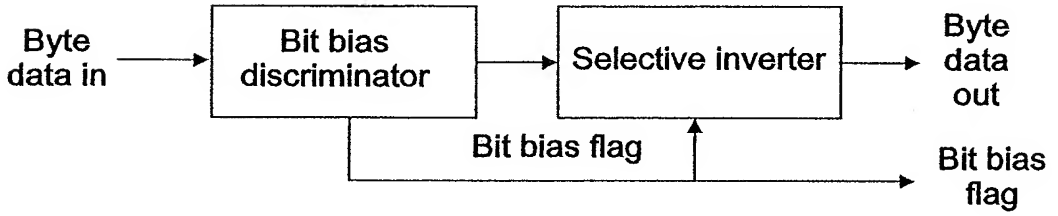
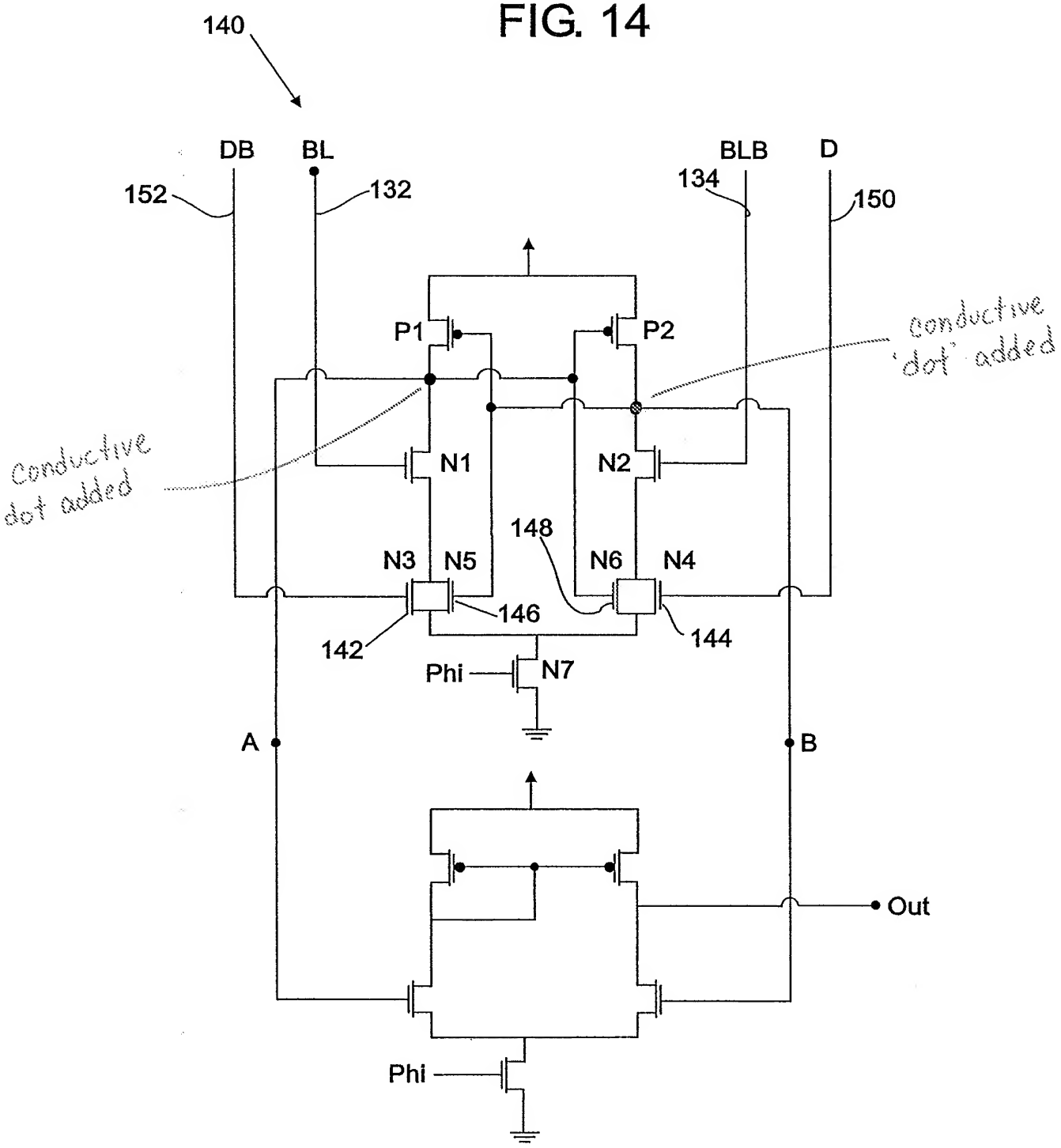


FIG. 14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Conductive dot added
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